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(54) Title: DIGITAL FILTERING SYSTEM
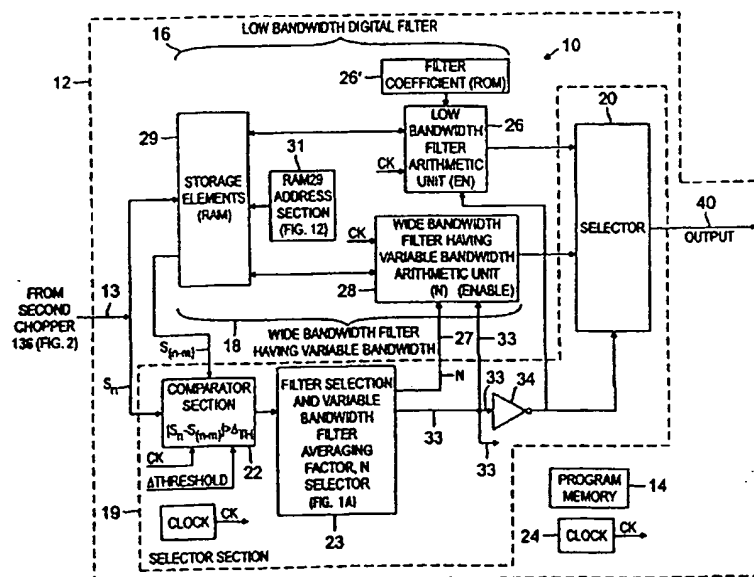
(57) Abstract

A digital filtering system (10) is fed by input signal and produces an output signal from either a relatively low bandwidth filter or a relatively wide bandwidth filter selectively in accordance with the time rate of change in the input signal. The output signal is produced by the relatively low bandwidth filter (26) when the input signal is slowly varying and the output signal is produced by the relatively wide bandwidth filter (28) when the input signal changes rapidly, after which the output is produced from the relatively low bandwidth filter when the input signal reverts to its more slowly varying characteristics.

DIGITAL FILTERING SYSTEM
Background of the Invention

5   This invention relates generally to digital
filtering systems and more particularly to digital
filtering systems having a bandwidth which varies as a
function of the time rate of change in an input signal
fed to the digital filtering system.

10   As is known in the art, a certain class of filter
design is a trade-off between the desire to remove noise
accompanying an input signal and to produce an output
signal which replicates the input signal itself. Thus,
while a reduction in the bandwidth of the filtering

15 system reduces noise, it also increases the response time
of the filter to changes in the input signal. For
example, in applications where there is a step change in
the input signal, while a low pass filter will reduce any
accompanying noise, as the bandwidth of the low pass

20 filter is reduced, the filter will also increase or
dampen the rise time of the output signal. One technique
suggested in U.S. Patent 3,755,750 to remove high
frequency noise is with a filtering system which operates
in one of two different modes. With such system, either

25 the input signal is coupled through a low bandwidth
filter, as when the input is slowly varying, or the low,
or narrow, bandwidth filter is in effect by-passed, as
when the input changes rapidly (i.e., when the input has
the characteristics or a square wave or step).

30   As is also known in the art, digital filters are
typically either Finite Impulse Response Filters (FIRs)
or Infinite Impulse Response Filters (IIRs). FIG. 9
shows a block diagram of a typical FIR digital filter.
The Z^{-1} boxes represent delay, or storage elements, with

35 the dots at the outputs of these boxes representing the

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stored value (state variable). The input is shown to
pass through R delay elements. The outputs of these
delay blocks and the current input are then multiplied by
coefficients, B_0-B_R, before being summed at the output.
5   Some of these coefficients may be zero. The output $y(n)$
is given by

$$Y(n) = B_0 \cdot u(n) + B_1 \cdot u(n-1) + B_2 \cdot u(n-2) + \ldots \ldots + B_R \cdot u(n-R)$$

Another type of filter is an IIR filter where the
current output depends also on previous outputs. This is
illustrated in FIG. 10. It is not necessary for the
10 number of delay elements storing $y(n)$ to equal the number
of delay elements storing $u(n)$. The output $y(n)$ for the
IIR is given by

$$y(n) = \sum_{k=1}^{R} A_k y(n-k) + \sum_{k=0}^{R} B_k u(n-k)$$

The following discussion is based around FIR
filters, however it is easily extended to cover IIR
15 filters. The overall frequency and transient response of
the filter is set by the values of the coefficients and
the number of delay elements present. To design a
filter, the passband frequency, stopband frequency,
passband ripple and stopband attenuation need to be
20 specified. Using these specifications the number of
coefficients in the filter and the values of the
coefficients can then be obtained. It is typically
necessary to increase the number of storage elements (R)
in order to meet demanding constraints on the filter
25 response. One such constraint that needs to be met in
many applications is a desire for low bandwidth. This
may be due to the need to reduce the effects of noise,

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since the noise outside the bandwidth of interest will be
attenuated. In order to meet a low bandwidth requirement
while having other characteristics such as a sharp roll-
off, and little ripple in the passband or stopband, the
5 number of coefficients needs to be increased.

Once the number of coefficients exceeds 1, there
is an inherent delay in the response time of the filter
to changes at its input. The old value of the input, (or
a value directly related to it), is retained in the
10 storage elements along the filter chain. When the input
changes to a new value, the contents of the storage
elements will initially be unaffected by the new input,
so only the first component of the output summation will
contain information about the new input value. The sum
15 is therefore performed with R terms that are based on the
old value of the input, and 1 term that takes into
account the new input value. The next output will be
based on R-1 old inputs and 2 new inputs. The output
therefore only slowly tracks changes in the input,
20 because for several outputs the output sum is more
heavily weighted towards the old input value. For a
symmetrical FIR filter, such as that illustrated in FIG.
9, with $B_0 = B_R$, $B_1 = B_{R-1}, ..$, then after $(R+1)/2$ inputs at
the new level the output will only be midway between the
25 old and new values. The output will not be fully settled
until R+1 inputs have occurred at the new level.

If a large number of coefficients are present,
then a change in the input will take a long time to
propagate to the output. This is undesirable in many
30 circumstances because changes at the input may need to be
detected as rapidly as possible. A filter with a wider
bandwidth would improve the time required to respond to
changes at the input, however this filter would typically
have a worse noise performance due to the wider

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bandwidth, and would therefore be unsuitable for that particular application.

Summary of the Invention

In accordance with the present invention, a
5   digital filtering system is fed by an input signal and produces an output signal from either a relatively low bandwidth digital filter or a relatively wide bandwidth digital filter selectively in accordance with the time rate of change in the level of the input signal.

10   With such an arrangement, the output signal is produced by the relatively low bandwidth digital filter when the input signal is slowly varying and the output signal is produced by the relatively wide bandwidth digital filter when the input signal changes rapidly,
15   after which the output is produced from the relatively low bandwidth digital filter when the input signal reverts to its more slowly varying characteristics. Thus, the filtering system provides a fast response to step changes at the input, while still having a low
20   bandwidth, low noise response when the input is steady. The low bandwidth filter can be optimized for noise performance and frequency response, while the wide bandwidth filter is optimized for response time.

In a preferred embodiment of the invention, the
25   relatively wide bandwidth digital filter processes the input signal with a varying bandwidth filter; the bandwidth being initially relatively wide and then steadily reducing until the digital filtering system reverts to processing the input signal with the
30   relatively low bandwidth digital filter.

In accordance with another feature of the invention, a digital filtering method is provided for producing an output signal from either a relatively low bandwidth digital filter or from a relatively wide

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bandwidth digital filter selectively in accordance with the time rate of change in the level of an input signal.

In a preferred embodiment, the relatively wide bandwidth digital filter processes the input signal
5 initially with relatively wide bandwidth and the bandwidth is reduced until the output signal is produced from the relatively low bandwidth digital filter.

Brief Description of the Drawing

Other features of the invention, as well as the
10 invention itself will become more readily apparent from the following detailed description taken together with the accompanying drawings, in which:

FIG. 1 is a block diagram of a digital filtering system according to the invention;
15   FIG. 1A is a block diagram of a filter selection and variable bandwidth filter averaging factor selector used in the digital filtering system of FIG. 1;

FIG. 2 is a block diagram of an analog to digital conversion system having the digital filtering system of
20 FIG. 1;

FIGS. 3A-3E are timing diagrams useful in understanding the operation of the analog to digital conversion system of FIG. 2;

FIG. 4 is a flow diagram of the steps used by the
25 digital filtering system of FIG. 1;

FIGS. 5A-5E are timing diagrams useful in understanding the digital filtering system of FIG. 1 and the method of FIG. 4;

FIGS. 6 through 8 are block diagrams of
30 alternative embodiments of the digital filtering system according to the invention;

FIG. 9 is a block diagram of a Finite Impulse Response Filter according to the prior art;

FIG. 10 is a block diagram of an Infinite Impulse
35 Response Filter according to the prior art;

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FIG. 11 is a block diagram of a clock disable circuit adapted for use with the digital filtering system of FIG. 1;

FIG. 12 is a block diagram of an address section
5   used in the filtering system of FIG. 1.

Description of the Preferred Embodiments

Referring now to FIG. 1, a digital filtering system 10 is shown. Such system 10 includes a digital processor 12 fed by an input signal on line 13. The
10 signal on line 13 is here a sequence of digital words (i.e., samples) produced by an analog to digital conversion system 15, described in copending patent application entitled "Analog to Digital Conversion System", Serial No.   , inventor Damien McCartney,
15 assigned to the same assignee as the present invention, filed concurrently herewith, the contents thereof being incorporated herein by reference. Here, the digital filtering system provides the function of the output filter 50 described in the above referenced copending
20 patent application.

More particularly, the analog to digital conversion system 15 is shown in FIG. 2 to include first chopper 112. The first chopper 112 has an input terminal 114 and an output terminal 116. The input terminal 114
25 is coupled to the output terminal 116 through two channels 118, 120, as shown. Each one of the channels 118, 120 includes a switch 122, 124, respectively, as shown. A train of binary signals (i.e., chop signals) is fed to the switches 122, 124 via line 126, as shown. The
30 train of binary signals on line 126 is shown in FIG. 3A. Thus, the train of binary signals has a period, T, as shown in FIG. 3A. It is noted that while line 126 is coupled directly to switch 124, line 126 is coupled to switch 122 through an inverter 128, as shown. Also, it
35 should be noted that an inverting, unity gain amplifier

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133 is serially connected between the input terminal 114
and the output terminal 116 in channel 124, as shown.

Thus, in operation, assume an analog signal, A_{IN},
is fed to input terminal 114. In response to one state
5 of the binary signal on line 126, here, when the binary
signal on line 126 is logic 0, during the first half of
each period, T, (i.e., during 0-T/2) switch 122 is closed
to pass the analog signal on input terminal 114 to output
terminal 116 without any change in polarity in the input
10 analog signal A_{IN}. During this first half of each period,
T, (i.e., during 0-T/2) switch 124 is in an open circuit
condition.   One the other hand, during the next half
period T/2 (i.e., from T/2 to T), when the binary signal
on line 126 changes to a logic 1, switch 122 is opened
15 and switch 124 is closed to thereby produce at output
terminal 116 during this half period from T/2 to T, the
input analog signal A_{IN} with reversed polarity, i.e., the
analog signal
$-A_{IN}$, because of inverting amplifier 133. Thus, the first
20 chopper 112 successively reverses the polarity of the
analog signal, A_{IN} at a rate, $R=2/T=2f_{CHOP}$. That is, the
first chopper 112 is responsive to the chop signal on
line 126 having the period T and passes the analog signal
A_{IN} to output 116 with non-reversed polarity (i.e., the
25 signal $+A_{IN}$) during a first portion of the period T and
with reversed polarity ($-A_{IN}$) during a second portion of
the period T, as shown in FIG. 3B.

A signal conditioning circuit 130 is fed by the
output 116 of the first chopper 112. The signal
30 conditioning circuit 130, for example an amplifier, is
fed by the signals produced by the first chopper 112 at
output 116 to produce corresponding analog signals at the
output 131 of circuit 130. Thus, the signal conditioning
circuit 130 is fed sequentially by the signals $+A_{IN}$ and -
35 A_{IN}, for producing with periodicity, T, a sequence of

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pairs of successive signals, $+A'_{IN}+V_{OSSC}$ and $-A'_{IN}+V_{OSSC}$, where V_{OSSC} is any offset voltage produced by the signal conditioning circuit 130. Thus, the signal conditioning circuit 130 is fed by the output of the first chopper 112

5   for producing a first conditioned signal, $+A'_{IN}+V_{OSSC}$, during the first portion of the period T and a second conditioned signal,

$-A'_{IN}+V_{OSSC}$, during the second portion of the period T.

An analog to digital converter (ADC) 132, here a
10 relatively high resolution ADC or sigma-delta modulator, as described in the above reference copending patent application, is provided for converting the analog signals produced by the signal conditioning circuit 130 at output 131 into sets of at least one digital word. In
15 the case of a relatively high resolution ADC, each set is one parallel N-bit digital word and in the case of a sigma-delta modulator each set is a sequence of low resolution, one- or two-bit, digital words. Assuming the former, the sets of digital words are produced by the ADC
20 at a rate, f_{OUT}, here at the rate R $=2/T$, as shown in FIG. 3C. As noted in FIG. 3C, an offset voltage, V_{OS}, corresponding to the total offset of the signal conditioning circuit and the analog to digital converter is also produced.

25   Thus, the ADC 132 produces a first digital word, $[+A'_{IN}+V_{OS}]|_{DIG}$, corresponding to the first conditioned signal, $+A'_{IN}+V_{OSSC}$, and produces a second digital word, $[-A'_{IN}+V_{OS}]|_{DIG}$, corresponding to the second conditioned signal, $-A'_{IN}+V_{OSSC}$, each one of such produced digital
30 words including therein the offset voltage, V_{OS}, as shown in FIG. 3C. That is, the digital words $[+A'_{IN}+V_{OS}]|_{DIG}$, $[-A'_{IN}+V_{OS}]|_{DIG}$, $\ldots$ are produced by the ADC 132 at a rate f_{OUT}. Here, $f_{OUT}=R$.

A second chopper 136 is fed by the digital words
35 $[+A'_{IN}+V_{OS}]|_{DIG}$ and $[-A'_{IN}+V_{OS}]|_{DIG}$, produced by the analog

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to digital converter at the rate f_{OUT}, and produces, with
the periodicity T, corresponding digital words
$[+A'_{IN}+V_{OS}]|_{DIG}$ and $[+A'_{IN}-V_{OS}]|_{DIG}$. Thus, the second
chopper 136 successively reverses at the rate R the

5   polarity of the digital words produced by the analog to
digital converter 132 on line 134. It is first noted
that the second chopper 136 is fed with the series of
digital words, on line 134. Thus, the second chopper 136
while functionally equivalent to the first chopper 112,

10   uses digital processing to provide its function.
However, for purpose of understanding, the second chopper
is functionally represented in FIG. 2 as having an input
terminal 138 and an output terminal 140. The input
terminal 138 is coupled to the output terminal 140

15   through two channels 142, 144, as shown. Each one of the
channels 142, 144 includes a switch 146, 148,
respectively, as shown. The train of binary signals is
fed to the switches 146, 148 via line 126, as shown. The
train of binary signals on line 126 is, as noted above,

20   shown in FIG. 3A. Thus, the train of binary signals has
a period, T, as shown in FIG. 3A. It is noted that line
126 is coupled to a delay 137. While the output of delay
137 is coupled directly to switch 148, the output of
delay 137 is coupled to switch 148 through an inverter

25   147, as shown. Also, it should be noted that an
inversion 149 is provided serially between the input
terminal 138 and the output terminal 140 in channel 144,
as shown. The delay 137 is provided to account for
conversion delay in the ADC 132. Here, the delay 137 in

30   the example shown in FIG. 3C is δ, as shown.

Thus, the second chopper 136 is a second switch
section, fed by the digital words $[+A'_{IN}+V_{OS}]|_{DIG}$ and $[-
A'_{IN}+V_{OS}]|_{DIG}$, and produces during each period, T, a pair
of corresponding digital words $[+A'_{IN}+V_{OS}]|_{DIG}$ and $[+A'_{IN}-
$

35   $V_{OS}]|_{DIG}$. That is, the second chopper 136 successively

reverses the polarity of the digital words produced by
the analog to digital converter 132 at the rate R.
Thus, in operation, digital words produced at the output
of ADC 132 corresponding to the first half of each period
5 T, i.e., from 0 to T/2, appear with a reversal in
polarity at output 140 of the second chopper 136, as
shown in FIG. 3D. On the other hand, corresponding to
the next half period T/2 (i.e., from T/2 to T), the
digital words produced at the output of ADC 132 appear
10 with a reversal in polarity at output 140 of the second
chopper 136, as shown in FIG. 3D.   To put it another
way, the second chopper 136 is responsive to the chop
signal on line 126 and passes to output 140 of the second
chopper 136 one of the produced first and second digital
15 words, $[+A'_{IN}+V_{OS}]|_{DIG}$, $[-A'_{IN}+V_{OS}]|_{DIG}$, with non-reversed
polarity, and passes to the output 140 the other one of
produced first and second digital words $[+A'_{IN}+V_{OS}]|_{DIG}$,
$[-A'_{IN}+V_{OS}]|_{DIG}$ with reversed polarity. For example,
referring to FIGs. 3C and 3D, here the digital words
20 $[+A'_{IN}+V_{OS}]|_{DIG}$ are passed to output 140 with non-reversed
polarity and the digital words $[-A'_{IN}+V_{OS}]|_{DIG}$ are passed
to output 140 with reversed polarity.

An output filter 150, here provided by the digital
filtering system 10 (FIG. 1), is fed by the output 140 of
25 the second chopper 136 and produces, on receipt of the
first produced digital word $[+A'_{IN}+V_{OS}]|_{DIG}$, a first
output digital word $A''_{IN}|_{DIG}$ and, on receipt of the second
produced digital word $[-A'_{IN}+V_{OS}]|_{DIG}$, a second output
digital word $A''_{IN}|_{DIG}$, with the offset voltage being
30 removed from each of such output digital words, as shown
in FIG. 3D. To put it another way, the output filter 150
is fed by the sequence of digital words $[+A'_{IN}+V_{OS}]|_{DIG}$
and $[+A'_{IN}-V_{OS}]|_{DIG}$, produced by the second chopper 136 at
output 140. The output filter 150 removes the $V_{OS}|_{DIG}$
35 portion of the sequence of digital words over a

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predetermined period of time. For purposes of
understanding, when referring to FIG. 3E, the digital
words $[+A'_{IN}+V_{OS}]|_{DIG}$, $[+A'_{IN}-V_{OS}]|_{DIG}$, produced by the
second chopper 136 at output 140 are filtered over 2T by
5 filter 150 to thereby remove the offset voltage $V_{OS}|_{DIG}$
components.

        While the chopper system has been discussed above
for a relatively high resolution ADC, a complete
discussion of a sigma-delta modulator system using
10 chopping is described in the above referenced copending
patent application entitled "Analog to Digital Conversion
System", inventor Damien McCartney, assigned to the same
assignee as the present invention, filed concurrently
herewith, the contents of which are incorporated herein
15 by reference.

        Referring now again to FIG. 1, as noted above, the
digital filtering system 10 performs the function of the
output filter 150 in FIG. 2. The processor 12 includes a
program memory 14 adapted to store a computer program
20 represented by the flow diagram shown in FIG. 4, a low
bandwidth digital filter 16, a wide bandwidth digital
filter 18 here having a variable bandwidth, a selector
section 19, and clock 24. The selector section 19
includes a selector 20, a comparator section 22, a filter
25 selection and variable bandwidth filter averaging factor,
N, selector 23 (shown in FIG. 1A) and an inverter 34.
The low bandwidth and wide bandwidth digital filters 16,
18 are here Finite Impulse Response (FIR) digital
filters. The filters 16, 18 have calculation modules or
30 arithmetic units 26, 28 which share storage elements,
here memory locations in random access memory (RAM) 29.
The memory locations are addressed by a RAM address
section discussed in detail in connection with FIG. 12.
Suffice it to say here, that the low bandwidth digital
35 filter arithmetic unit 26 and the wide bandwidth digital

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filter arithmetic unit 28 are enabled (EN) are different
times. The enable (EN) of arithmetic unit 28 is coupled
directly to selector 23 whereas the enable (EN) of
arithmetic unit 26 is shown coupled to selector 23
5 through the inverter 34. Thus, here, either the low
bandwidth digital filter 16 or the wide bandwidth digital
filter 18 will be enabled by the binary signal produced
on line 33 by the selector 23.

Here, low bandwidth digital filter 16 has a fixed
10 bandwidth and performs a full FIR convolution, involving
multiplications and summations over a predetermined
number, here over 22 input signal samples on line 13
stored in 22 storage locations in RAM 29. That is, low
bandwidth digital filter 16 is here a 22 coefficient
15 symmetrical low bandwidth FIR digital filter. The
coefficients, "B" (FIG. 9), used by the arithmetic unit
are stored in a read only memory (ROM) 26'.

Here, the wide bandwidth digital filter 18 has a
variable bandwidth. That is, as will be described, when
20 enabled in response to comparator section 22 detecting a
step change in the input signal on line 13, the wide
bandwidth filter 18 averages the samples by an increasing
number of samples and thereby correspondingly reduces its
bandwidth in accordance with data fed thereto by the
25 selector 23 on bus 27. Here, the wide bandwidth digital
filter 18 uses up to 16 input signal samples (i.e.,
digital words) in producing a corresponding output
digital word. Thus, the wide bandwidth digital filter 18
uses the same 22 storage locations in RAM 29 as the low
30 pass digital filter 16; however the wide bandwidth
digital filter 18 will only use, at most, the 16 most
recent samples. The wide band digital filter 18 is here
also a FIR digital filter.

In operation, the digital filtering system 10 is
35 fed by an input signal on line 13 (i.e., the output on

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line 140 of the second chopper 136 (FIG. 2)) and produces
an output signal on line 40 from either the relatively
low bandwidth digital filter 16 or the relatively wide
bandwidth digital filter 18 selectively in accordance
5　with the time rate of change in the input signal on line
13. More particularly, the output signal on line 40 is
produced by the relatively low bandwidth digital filter
16 when the input signal on line 13 is slowly varying and
the output signal on line 40 is produced by the
10　relatively wide bandwidth filter 18 when the input signal
on line 13 changes rapidly, after which the output on
line 40 is produced from the relatively low bandwidth
filter 16 when the input signal reverts to its more
slowly varying characteristics.

15　　　　As described in connection with FIGS. 2 and 3A-3E,
the input to filtering system 10 will be a digital word
representing a sampled analog signal plus an offset
voltage (i.e. $[A'_{IN}+V_{OS}|_{DIG}]$) and a succeeding sample of
the analog signal will be a digital word representing a
20　sampled analog signal minus an offset voltage (i.e. $[A'_{IN}-V_{OS}|_{DIG}]$), where A'_{IN} is a digitalized input signal sample
and V_{OS} is the total offset voltage from the ADC and/or
any signal conditioning circuitry between a first chopper
and a second chopper. The filtering system 10 will
25　remove this polarity varying offset voltage (i.e., $+V_{OS}$, $-V_{OS}$) and thereby produce a series of outputs $A''_{IN}|_{DIG}$ with
V_{OS} removed.

　　　　A comparison is made by subtracting a sample S_{n-m}
from sample S_n at each clock pulse CK. These samples are
30　stored in RAM 29. Thus, the comparison is made between a
current input signal sample S_n and a previous input
signal sample, S_{n-m}, where here m=2 (i.e., the comparison
is made between two $[A'_{IN}+V_{OS}|_{DIG}]$ terms or two $[A'_{IN}-V_{OS}|_{DIG}]$ terms so that the offset is not seen as a step
35　change. More particularly, the comparison is made by

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subtracting the sample S_{n-m} from the sample S_n at each clock pulse, CK. If the absolute difference $|S_{n-m}-S_n| = \Delta$ is greater than a predetermined reference threshold, $\Delta_{THRESHOLD}$, then it is deemed that a step change has

5   occurred in the input signal. In such case, the wide bandwidth filter 18 is selected by the selector section 23 setting active a "step change" flag; here raising the level of line 33. As noted above, the wide bandwidth filter 18 is a variable bandwidth filter. It starts off

10   as an average by 2 and increases by a factor of 2 in a manner to be described. (It should be noted that if chopping is not performed, it starts off as an average by 1). Thus, in general, an averaging factor starts off as an averaging factor, N_0, and then successively increases)

15   as described.

More particularly, whenever an input signal on line 13 is applied to the digital filtering system 10, the comparator section 22, which is fed by line 13, makes the comparison described above. If a step change in the

20   input signal is deemed to have occurred in the input signal, the wide bandwidth filter 18 is enabled to an appropriate averaging factor, (i.e., bandwidth) and the "step change" flag (line 33) is set active. If no step change is deemed to have occurred in the input signal,

25   then a check is made to determine whether the wide bandwidth filter 18 or low bandwidth filter 16 is currently selected based on previous calculations. If the low bandwidth filter 16 is selected (i.e., there is not a step change in the input signal currently being

30   filtered by the wide bandwidth filter 18), the low bandwidth filter 16 is enabled and its output is used as the output of the digital filtering system 10. If, on the other hand, the wide bandwidth filter 18 is actively processing the input signal, then an averaging is

35   performed by the wide band filter using the then current

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averaging factor (i.e., the then current bandwidth of the wide bandwidth filter).

The averaging factor of the wide bandwidth filter 18 starts off at 2, as noted above, and is then increased

5   in powers of 2 to 4, 8, 16 ... to allow the wide bandwidth filter 18 to steadily reduce its bandwidth and thereby become more accurate as more input samples become available. More particularly, after averaging with the initial wide bandwidth filter 18 bandwidth, a check is

10   made to determine if more averages remain to be performed using the current averaging factor (i.e. bandwidth), or whether there are now sufficient input samples at the new level to produce the output of the digital filtering system 10 using the next averaging factor (i.e., the next

15   lower bandwidth of the wide bandwidth filter 18). If there are more averagings to be performed, (i.e., more digital filtering with the current bandwidth) the "averages remaining" to be performed is decremented (i.e., the count in the "averages remaining" counter 210

20   will be decremented) until it reaches zero. When the "averages remaining" count in counter 210 reaches zero, the next output will be produced with the current averaging factor and the "averages remaining" counter 210 is interrogated and the averaging factor is advanced,

25   (i.e., incremented), to the next averaging factor thereby again reducing the bandwidth of the wide band filter 18. If this new averaging factor is a predetermined factor corresponding to the narrowest bandwidth of the wide bandwidth filter 18, this implies that there are now

30   sufficient samples for the low bandwidth filter 16 processing. In such case, the "step change" flag, (i.e., the binary signal on line 33) is deactivated (i.e., cleared) the output of the digital filtering system 10 on line 40 will be performed using the low bandwidth filter

38 until another step change is deemed to have occurred
in the input signal.

It should be noted, that because the input signal
on line 13 is being continually examined by the
5 comparator section 22, it is possible to detect that a
step change in the input signal occurs while the previous
step change has not yet settled sufficiently for low
bandwidth filter 16 processing (i.e., a step change in
the input signal occurs while the "step change" flag
10 (i.e., the binary signal on line 33) is active. In such
case, the wide bandwidth filter 18 recommences performing
the average by 2 operation even if it had been performing
an average by some other factor. To put it another way,
the wide bandwidth filter 18 reverts to its widest
15 bandwidth even if it was processing the input signal with
a lower bandwidth.

The change from one averaging factor to another
factor (i.e., the change from one bandwidth to a lower
bandwidth) occurs automatically when there are sufficient
20 input samples to perform an average by N with N input
samples at the new level. For example, the wide
bandwidth filter 18 advances from an average by 4 to an
average by 8 once there are 8 input samples that have
exceeded the step threshold comparison (it being noted
25 that the average by 8 occurs after 9 samples at the input
level due to the comparison being made to the input two
previous). This means that there will be four outputs
produced at the digital filtering system 10 on line 40
using an average by 4. Once the next input sample
30 arrives, there will now be enough data to perform an
average by 8 and 8 samples are produced with an average
by 8. Thus, here the wide bandwidth filter 18 uses 16
input samples and produces 22 outputs after the input
reaches a substantially constant level before reverting

to the low bandwidth filter (i.e., changes from sample to sample less than $\Delta_{THRESHOLD}$).

Thus, referring to FIG. 4, in Step 50, a current sample, S_n, of the input signal on line 13 is acquired by
5 the digital filtering system 10. In response to a subsequent clock pulse on line CK, comparator section 22 compares the level of the current sample S_n with the previous sample, S_{n-m}, where in this example m=2, Step 52. Thus, here a comparison is made between $\Delta=|S_{n-2}-S_n|$) and a
10 predetermined threshold difference $\Delta_{THRESHOLD}$ by comparator section 22, Step 54. If the difference in level between S_n and S_{n-2} (i.e., $\Delta=|S_{n-2}-S_n|$) is greater than the predetermined threshold difference $\Delta_{THRESHOLD}$, a step change is deemed to have occurred in the input signal:
15 (1) the averaging factor for the wide bandwidth filter 18 is initialized, here to 2 (i.e., the wide bandwidth filter is set to its widest bandwidth); (2) the "averages remaining" is initialized, here to 2; and (3) the "step change" active software flag is produced by the selector
20 section 19 (i.e., the selector 23 enables the wide bandwidth digital filter arithmetic unit 28 and disables the low bandwidth digital filter arithmetic unit 26 (here represented by the binary signal on line 33), Step 55.

Thus, referring to an example shown in FIGS. 5A-
25 5D, where m=2, samples S_1, S_2 and S_3 of the input signal (FIG. 5C) are equal, here equal to zero. Thus, from Step 54, $\Delta<\Delta_{THRESHOLD}$. In such case, the digital filtering system 10 determines whether the "step change" flag is active (i.e., whether the signal on line 33 is at a low
30 level or a high level). Here, such flag not being active results in the low bandwidth filter 16 producing the output on line 40 as indicated in Step 57.

When sample S_4, here 0.5, is acquired, Step 50, from Step 52, $S_4-S_2=\Delta=0.5$. Thus, because the difference Δ
35 has a level greater than the predetermined threshold

level, here $\Delta_{THRESHOLD}$ = 0.1, from Step 54, system proceeds
with Step 55. In Step 55, and referring also to FIG. 1A,
the state of the control signal produced by comparator 22
changes thereby loading a predetermined value, here 1,

5 stored in register 200 into "averaging factor" up-counter
202. The contents of the "averaging factor" up-counter
202, M, is decoded by decoders 204, 206 and 208. Decoder
204 detects that the contents of counter 202 is no longer
5 and therefore raises the level on line 33, i.e.,

10 produces a flag. The decoder 206 decodes the 1 stored
"averaging factor" up-counter 202 and produces the
averaging factor, N, here N=2, on bus 27. The decoder
208 decodes the 1 stored in counter 202 and produces the
"average remaining" number AR, here 2, which is loaded

15 into "averages remaining" down-counter 210 as the signal
produced by section 22 is passed through OR gate 212 to
the load LD terminal of counter 210. Thus, the averaging
factor, N, is initialized to 2 (FIG. 5C); the "averages
remaining" , AR, stored in counter 210 is initialized to

20 2 (FIG. 5B); and the "step change" flag (line 33) is set
active (FIG. 5A) so that the wide bandwidth digital
filter arithmetic unit 28 is enabled and the low
bandwidth digital filter arithmetic unit 26 is disabled,
Step 55. The digital filtering system 10 proceeds to

25 Step 58. The digital filtering system 10 performs, in
accordance with Step 58 the average by 2 here
$S_4'=(S_4+S_3)/2$ =0.25 as shown in FIG. 5D, Step 58. It is
noted that a clock pulse is produced for counter 202 only
when the contents of counter 210 returns to 0 and then

30 only after a one clock pulse delay provided by delay 211.
Thus, the contents of counter 202 remains at 1 and N
remains at 2.

      The next sample, S_5, here 1, is acquired as shown
in FIG. 5C. Again, Step 52 determines $\Delta>\Delta_{THRESHOLD}$. The

35 "averaging factor" up-counter 202 is again, in accordance

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with Step 55, initialized to 1 so that again N=2 to set
wide bandwidth filter 18 to the widest bandwidth for this
chop mode, i.e., here the average factor, N, is again set
to 2, as shown in FIG. 5B and the "average remaining"
5 counter 210 is again initialized to 2. The "step change"
flag (line 33) remains set, i.e., active. The process
proceeds again to Steps 58, 60, 61 and the output $S'_5 =$
$(S_5 + S_4)/2$ is produced by the digital filtering system 10,
Step 62. It is noted that Step 61 decrements the
10 "average remaining" to 1 (FIG. 5B).

        The next sample, S_6, is taken. Since the
difference between S_6 and S_4 is again greater than
$\Delta_{THRESHOLD}$, and the process described above repeats with N
and AR both initially equal to 2.

15   The next sample S_7, here having the same level as
S_5, is acquired as shown in FIG. 5C. Step 52 determines
$\Delta < \Delta_{THRESHOLD}$. A check is made in Step 56 if the existing
"step change" flag is active. Because the "step change"
flag has not been deactivated, it is still active as
20 shown in FIG. 5A. Thus, the averaging is performed with
the current averaging factor, which is still 2; as noted
above, however here the comparator section 22 does not
detect a difference $\Delta > \Delta_{THRESHOLD}$ and therefore the "average
remaining" counter 210 is not initialized to 2, so it
25 remains at 1 from Step 61 for sample S_6. It is noted
that Step 61 decrements the "averages" remaining counter
to 0 (FIG. 5B). The process proceeds again to STEPs 58,
60, 61 and the output $S_7' = (S_7 + S_6)/2$ is produced by the
digital filtering system 10 (Step 62).

30   The next sample S_8, here having the same level as
S_6, is acquired as shown in FIG. 5C. Thus, Step 54
indicates that $\Delta < \Delta_{THRESHOLD}$. A check is made in Step 56 if
the existing "step change" flag is active. Because the
"step change" flag has not been deactivated, it is still
35 active as shown in FIG. 5A. Thus, the averaging is

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performed with the current averaging factor, N, which is still 2; as noted above, however, the "average remaining" counter 210 was decremented to 0 in Step 61 for sample S_7. The averaging produces an output sample

5   $S'_8=(S_8+S_7)/2$, Step 58. Thus, from Step 60, a determination is made that the digital filtering system 10 has completed processing with the current, here 2, averaging factor. Thus, from Step 64, the system changes the wide bandwidth filter 18 to the next lower bandwidth

10 by using an increased averaging factor of N=4, as shown in FIG. 5B for the next acquired sample, S_9. Also, the number of "averages remaining" counter 210, as noted above, is set, here to 3, as shown in FIG. 5C, Step 66. Here, the averaging factor of the low bandwidth filter is

15 22. Thus, from Step 68, because the averaging factor is now 4 and therefore not equal to 22, Step 70, the result S_8' is output (Step 69').

The process repeats, it being noted from FIGS. 5A-5D: samples S_9', S_{10}', S_{11}' and S_{12}' are produced using

20 averages of 4 samples; input sample S_{13} results in the average factor increasing from 4 to 8, with the "average remaining" being initialized to 7; input sample S_{21} results in the average factor increasing from 8 to 16, with the "average remaining" being initialized to 5; and

25 sample S_{26} results in the step 68 indicating that the "step change" flag, line 33 (FIG. 5A) should be changed as in Step 70 with the result that the low bandwidth filter 16 produces the output samples on line 40 (FIG. 1) for subsequent samples until another step change. Output

30 S_{26}' is the last output to be produced using the wide bandwidth filter 18 (Step 69), while output S_{27}' is the first output to be produced with the low bandwidth filter after the change in input has occurred.

The process is summarized in the following TABLE:

TABLE

Sample	Output Section 22	Counter 202, M	Decoder 204, Line 33	Decoder 206, N	Counter 210, AR
S_1	$\Delta < \Delta_{TH}$	5	LOW	22	0
S_2	$\Delta < \Delta_{TH}$	5	LOW	22	0
S_3	$\Delta < \Delta_{TH}$	5	LOW	22	0
S_4	$\Delta > \Delta_{TH}$	1	HIGH	2	2
S_5	$\Delta > \Delta_{TH}$	1	HIGH	2	2
S_6	$\Delta > \Delta_{TH}$	1	HIGH	2	2
S_7	$\Delta < \Delta_{TH}$	1	HIGH	2	1
S_8	$\Delta < \Delta_{TH}$	1	HIGH	2	0
S_9	$\Delta < \Delta_{TH}$	2	HIGH	4	3
S_{10}	$\Delta < \Delta_{TH}$	2	HIGH	4	2
S_{11}	$\Delta < \Delta_{TH}$	2	HIGH	4	1
S_{12}	$\Delta < \Delta_{TH}$	2	HIGH	4	0
S_{13}	$\Delta < \Delta_{TH}$	3	HIGH	8	7
S_{14}	$\Delta < \Delta_{TH}$	3	HIGH	8	6
S_{15}	$\Delta < \Delta_{TH}$	3	HIGH	8	5
S_{16}	$\Delta < \Delta_{TH}$	3	HIGH	8	4
S_{17}	$\Delta < \Delta_{TH}$	3	HIGH	8	3
S_{18}	$\Delta < \Delta_{TH}$	3	HIGH	8	2
S_{19}	$\Delta < \Delta_{TH}$	3	HIGH	8	1
S_{20}	$\Delta < \Delta_{TH}$	3	HIGH	8	0
S_{21}	$\Delta < \Delta_{TH}$	4	HIGH	16	5
S_{22}	$\Delta < \Delta_{TH}$	4	HIGH	16	4
S_{23}	$\Delta < \Delta_{TH}$	4	HIGH	16	3
S_{24}	$\Delta < \Delta_{TH}$	4	HIGH	16	2

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S_{25}	$\Delta < \Delta_{TH}$	4	HIGH	16	1
S_{26}	$\Delta < \Delta_{TH}$	4	HIGH	16	0
S_{27}	$\Delta < \Delta_{TH}$	5	LOW	22	0

Referring now to FIGS. 6 through 8, alternative
embodiments of the digital filtering system 10, are
shown. Thus, in FIG. 6 the digital filters 16, 18 in
digital filtering system 10' each includes its own
storage elements 29_1, 29_2, respectively. Here, the input
samples are stored in each storage element of the filters
16, 18. The computation of each filter 16, 18 is then
performed. The computation of both filters 16, 18 may be
performed in parallel using separate arithmetic units, or
sequentially using a single arithmetic unit. The output
of one of the filters 16, 18 is then selected, depending
on the "step change" flag condition produced by
comparator section 22.

In FIG. 7, another alternative embodiment of the
digital filtering system 10" uses independent storage
elements 29_1, 29_2 for each of the filters 16, 18, as in
the system shown in FIG. 6. Here, as in FIG. 1, the
computation is performed at any one time by only one of
the filters 16, 18. As in FIG. 1, the one of the filters
16, 18 producing the digital filtering system 10" output
is selected by the comparator section 22.

Another alternative embodiment of the digital
filtering system 10''' is shown in FIG. 8. The digital
filtering system 10''' uses common stage elements 29.
The wide bandwidth filter 18 may not use all these
storage elements in calculating its output. The
computation of filters 16, 18 is performed using either a
shared arithmetic unit or separate arithmetic units. One
of the filters 16, 18 is selected to provide the system
output in accordance with comparator section 22.

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It should be noted that if filters 16, 18 are
Infinite Impulse Response (IIR) filters, the output of
each one of the filters 16, 18 would also have to be fed
back to the storage elements. Therefore, the digital
5 filtering systems 10, 10'" described in FIGS. 1 and 8
would be unsuitable for IIR implementations because they
require shared storage elements and, in general, filter
16 and filter 18 would not produce identical results so
that the filters 16, 18 could not share the storage
10 elements 29 that record previous outputs since the
outputs would be different for each of the filters 16,
18.

Referring now to FIG. 11, a circuit is shown for
preventing outputs from being produced (by, in effect,
15 disabling the clock 24 (FIG. 1)) until there have been a
predetermined minimum number of samples produced by ADC
132 (FIG. 2). (Here, the disabling of clock 24 is
effected by, during execution of the program stored in
the program memory 14, examining the value of down-
20 counter 306, to be described, and if it equals zero, then
the program continues through the filter program
execution while if it is not zero the computer program
does not execute the filtering program sequence).

Here, digital samples are produced by ADC 132 at a
25 rate, f_{OUT}. In response to a change on line 300, an event
change detector 304 included in the selector section 19
(FIG. 1) produces a LOAD signal for down-counter 306.
(The change on line 300 may be caused from, for example,
"power-up" of the analog to digital conversion system of
30 FIG. 2 or when the ADC 132 is to receive an input from a
different channel (i.e., A or B) via a change in a
control signal on line 300 to multiplexer 302;
hereinafter collectively referred to as an event). In
response to such LOAD signal, i.e., the detected event,
35 counter 306 is preset to the value stored in register

- 24 -

308. The value in register 308 repr sents the number of samples which must be produced by the ADC 132 after the detected changed condition by event detector 304 before enablement of clock 24. Thus, here register 308 stores a
5 value 2 and the clock 24 (FIG. 1) will be enabled only after 2 samples have been produced by ADC 132.

More particularly, and referring also to FIG. 12, the RAM 29 address section 31 includes an address counter 400, an address offset section 402, an adder 404 fed by
10 the outputs of the counter 400 and address offset section 402, and a "modulo 22" arithmetic 406 fed by the adder 404 for producing the addresses for RAM 29 (FIG. 1). In operation, counter 400 provides a"base" address for the RAM 29. The counter 400 is incremented in response to
15 each new sample fed to the filter 12 (FIG. 1). Counter 400 operates modulo-22. That is, when the contents of counter 400 reaches 22, the contents are reset to 0 and the process repeats. Therefore, the outputs produced by counter 400 are 0, 1, 2,... 21. It is also noted that
20 the output of event change detector 304 (FIG. 11) is fed to the reset input of counter 400.

Offset section 402, in response to signals fed thereto during execution of the program stored in program memory 14, provides an output which is to be added or
25 subtracted from the "base" address provided by the counter 400 in adder 404. The amount to be added or subtracted varies depending on whether the low bandwidth filter 16 (FIG. 1) or the wide bandwidth filter 18 is being used to provide the filter 12 (FIG. 1) output. For
30 example, offset section 402 produces an offset address of -2 to extract data from a RAM 29 location 2 previous to the current address as where the second previous sample, S_{n-m} is to be subtracted from the current sample, S_n, where m=2, in comparator section 22 (FIG. 1). Thus, the
35 offset network produced -2 is added to the "base" address

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produced by counter 400, to provide the address for RAM
29.

Considering now the operation of the address
section 31 in connection with the event change detector
5 304 (FIG. 11), here samples occurring prior to a detected
event change by change detector 304 are indicated by S_q,
S_{q-1}, S_{q-2}, ... and samples occurring after a detected
event change by change detector 304 are indicated, as
discussed above in connection with FIGS. 4 and 5A-5E, S_1,
10 S_2, ...S_{n-1}, S_n. Thus, considering a first input S_q
occurring before the change occurs on line 300 for
multiplexer 302 (FIG. 11). The RAM address section 31
writes sample S_q into some address "p". After writing
such sample S_q into address "p", the write address (i.e.,
15 counter 400, is incremented to an address "p+1". The
comparison section 22 (FIG. 1) operates to compute $\Delta=|S_{q-2}-S_q|$ and produce a signal on line 33 in accordance with
the relationship between Δ and $\Delta_{THRESHOLD}$, as described
above.

20   When an event is detected by the change detector
304, here a change in the channel selected by the control
signal on line 300, the RAM 29 in response to the event
detect signal produced by detector 304 presets the data
in all RAM 29 locations to a predetermined default value.
25 The predetermined value is sufficiently smaller than the
values expected for the samples to be fed to the digital
filtering system 10 minus $\Delta_{THRESHOLD}$, for reasons to be
discussed. Further, the detected event initializes the
RAM address counter 400 (FIG. 12) to 0 and causes counter
30 306 (FIG. 11) to be initialized to 2, as described above,
to disable clock 24 (FIG. 1). It is also noted that
because the clock 24 is disabled, the comparison section
22 (FIG. 1) is set to 0 and no comparison is performed.

The first sample after the channel change, S_1,
35 then arrives. This sample is written into RAM location

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0. The other RAM locations are still at the default value. The counter 306 is decremented to 1, however the clock 24 is still disabled so again no comparison is performed by section 22. There is no output produced by
5 the digital filtering system 10 because the clock 24 is disabled.

The next sample, S_2, arrives and is written into RAM location 1. Counter 306 is decremented to 0, re-enabling the clock 24. A comparison is therefore performed by
10 section 22 as described above in connection with FIGS. 4 and 5A-5E between the current sample, S_2 and the sample two previous. This is achieved by reading from the current RAM 29 (i.e. location (1) from counter 400) and subtracting the data from the location 2 previous; (i.e.,
15 location (1-2=-1) by offset section 402 and adder 404). Thus, modulo 406 produces an address 21, i.e., the last location in RAM 29. The comparison is therefore performed between the contents of location 1 and the contents of location 21 (i.e., between sample S_2 and the
20 predetermined default value. Because the default value is smaller than the smallest expected sample to be fed to the filtering system minus $\Delta_{THRESHOLD}$, the comparison result performed by section 22 will always result in an indication that the threshold $\Delta_{THRESHOLD}$ has been exceeded.
25 Therefore, the averaging factor, N. and average remaining counter 210 (FIG. 1A) are initialized as described above in connection with FIG. 1A and the wide bandwidth filter 18 is selected. as described above. An average by two is performed on samples S_1 and S_2. The first output after
30 the channel change by multiplexer 302 is therefore produced after two input samples.

The next sample S_3 then arrives and is written into RAM location (2). Counter 306 is still 0 so that the clock 24 is enabled. A comparison is made in section
35 22 between sample S_1 and sample S_3. The result of this

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comparison will depend on the levels of such samples as described above. The process continues and eventually all locations in RAM 29 will have data written into them so that the "base" address produced by counter 400 will
5 wrap-around to 0 and sample S_1 will be overwritten with new data. Thus, the wide bandwidth filter having variable bandwidth 18 is selected in accordance with the time rate of change in the level of the input signal or a detected event.

10   As more input samples are acquired, the bandwidth of the wide bandwidth filter will reduce, provided the input samples remain within a threshold of each other, until the low bandwidth digital filter 16 is selected, as described above. Thus, once the comparison section 22
15 indicated that the threshold $\Delta_{THRESHOLD}$ has been exceeded either because of the time rate of change in actual samples fed to the filtering system or by an change in event which provides data to the comparison section 22 indication that the threshold $\Delta_{THRESHOLD}$ has been exceeded
20 the action of the selection section 19 proceeds as described above in connection with FIG, 4 and 5A-5E. That is, the variable bandwidth filter processes the input signal with a varying bandwidth, the bandwidth being relatively wide in response to a relatively high
25 time rate of change in the level of the input signal or the detected event and then reducing to a lower bandwidth once the time rate of change is relatively low.

        The digital filtering system 10 can therefore produce a correct output after only two input samples
30 after an event, while a standard 22 coefficient FIR could require 22 input samples after an event before producing a correct output.

        Other embodiments are within the spirit and scope of the appended claims. For example, the wide bandwidth
35 filter 18 need not be variable in bandwidth but may be a

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filter with a fixed number of coefficients. If a
variable filter is used, other averages may be used, for
example, 1, 2, 3, 4, ... 22. Further, a status bit, from
the "step change" flag, may be provided to indicate
5 whether the input is settled or not. Still further, the
digital filtering system 10 may take differences between
successive samples (i.e., m=1) in applications where
chopping is not used and may also use an initial
averaging factor, N, of 1 and average remaining of 0, in
10 response to a step.

What is claimed is:

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1.   A digital filtering system, comprising:
a relatively low bandwidth filter adapted for
coupling to an input signal;
a relatively wide bandwidth filter adapted for
5 coupling to the input signal;
a selector section for producing an output signal
from either the relatively low bandwidth filter or the
relatively high bandwidth filter selectively in
accordance with the time rate of change in the level of
10 the input signal.

2.   A digital filtering system, comprising:
a relatively low bandwidth digital filter adapted
for coupling to an input signal;
a variable bandwidth digital filter adapted for
15 coupling to the input signal;
a selector section for producing an output signal
from either the relatively low bandwidth filter or the
variable bandwidth filter selectively in accordance with
the time rate of change in the level of the input signal.

20   3.   The digital filtering system recited in claim
2 wherein the variable bandwidth filter processes the
input signal with a varying bandwidth, the bandwidth
being relatively wide in response to a relatively high
time rate of change in the level of the input signal and
25 then reducing to a lower bandwidth once the time rate of
change is relatively low.

    4.   The digital filtering system recited in claim 2 wherein the filtering system processes a sequence of samples of the input signal, and wherein the selector section includes a comparison section for determining the

5 difference in levels between pairs of samples, the selector section selecting either the relatively low bandwidth filter or the variable bandwidth filter selectively in accordance with the determined difference relative to a threshold level.

10   5.   The digital filtering system recited in claim 4 wherein the selector section selects the variable bandwidth filter when the determined difference is greater than the threshold level.

    6.   The digital filtering system recited in claim 15 4 wherein the selector section varies the bandwidth of the variable bandwidth filter, such bandwidth being relatively wide when the determined difference is greater than the threshold level and then reducing to a lower bandwidth once the determined difference is less than the 20 threshold level.

    7.   The digital filtering system recited in claim 5 wherein the low bandwidth filter is an FIR filter having a predetermined number of coefficients and wherein the selector section selects the low bandwidth filter 25 once a predetermined number of samples have been fed to the filtering system with the determined difference below the threshold level.

    8.   The digital filtering system recited in claim 7 wherein the predetermined number of samples is equal to 30 the predetermined number of coefficients minus one.

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9. A digital filtering system for filtering samples of an input signal, comprising:

a low bandwidth filter;

a variable digital filter, such filter being a
5　moving average filter having a variable averaging factor N;

a selector section for producing an output signal from either the low bandwidth filter or the variable digital filter selectively in accordance with a
10　determined difference in level between a pair of samples relative to a threshold level, such selector section varying the averaging factor N, the averaging factor N being N_0 when the determined difference is greater than the threshold level and is then successively increased
15　once the determined difference is less than the threshold level.

10. The system recited in claim 9 wherein N_0 is 2.

11. The system recited in claim 9 wherein N_0 is
20　1.

12. The system recited in claim 10 wherein N is successively increased by factors of 2 to 2^i once (2^i-1) samples have been fed to the digital filter with the determined difference less than the threshold level.

25　13. The system recited in claim 11 wherein N is successively increased by factors of 2 to 2^i once (2^i-1) samples have been fed to the digital filter with the determined difference less than the threshold level.

14. The system recited in claim 9 wherein the selector section produces an output signal indicating when the variable filter is selected.

15.   An analog to digital conversion system,
5 comprising:

a first chopper, responsive to a chop signal having a period T, for passing an analog signal to an output with non-reversed polarity during a first portion of the period T and with reversed polarity during a
10 second portion of the period T;

an analog to digital converter for producing digital words corresponding to the signals passed by the first chopper, each one of such produced digital words including therein an offset voltage;

15   a second chopper, responsive to the chop signal, for passing to an output of the second chopper the produced digital words with non-reversed polarity or with reversed polarity selectively in accordance with the chop signal; and,

20   a digital filter, fed by the output of the second chopper, for removing the offset voltage, such digital filter comprising:

a relatively low bandwidth filter section fed by the second chopper;

25   a relatively wide bandwidth filter section fed by the second chopper;

and a selector section for producing an output signal from either the relatively low bandwidth filter or the relatively high bandwidth filter
30 selectively in accordance with the time rate of change in the level of the digital words produced by the second chopper.

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16.   An analog to digital conversion system,
comprising:

a first chopper, responsive to a chop signal
having a period T, for passing an analog signal to an
5   output with non-reversed polarity during a first portion
of the period T and with reversed polarity during a
second portion of the period T;

an analog to digital converter for producing
digital words corresponding to the signals passed by the
10   first chopper, each one of such produced digital words
including therein an offset voltage;

a second chopper, responsive to the chop signal,
for passing to an output of the second chopper the
produced digital words with non-reversed polarity or with
15   reversed polarity selectively in accordance with the chop
signal; and,

a digital filter, fed by the output of the second
chopper, for removing the offset voltage, such digital
filter comprising:

20   a relatively low bandwidth filter section fed
by the second chopper;

a variable bandwidth filter section fed by
the second chopper;

and a selector section for producing an
25   output signal from either the relatively low bandwidth
filter or the variable bandwidth filter selectively in
accordance with the time rate of change in the level of
the digital words produced by the second chopper.

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17. The system recited in claim 16 wherein the digital filter processes a sequence of samples produced by the second chopper, one set of such produced samples including therein the offset voltage with a first
5 polarity and another second set including therein the offset voltage with a reversed polarity, wherein the selector section includes a comparison section for determining the difference in level between pairs of samples, each one of such samples in the pair being from
10 the same set, the selector section selecting either the relatively low bandwidth filter or the variable bandwidth filter selectively in accordance with the determined difference relative to a threshold level.

18. A digital filtering system for filtering
15 samples of a input signal fed thereto, comprising;
      a moving average filter having a variable averaging factor N;
      a control section for varying the variable averaging factor N in accordance with a determined
20 difference in level between a pair of the samples relative to a threshold level, the averaging factor N being N_0 when the determined difference is greater than the threshold level and is then successively increased once the determined difference is less than the threshold
25 level.

19. The system recited in claim 18 wherein N_0 is 2.

20. The system recited in claim 18 wherein N_0 is 1.

21. The system recited in claim 19 wherein N is successively increased by factors of 2 to 2^i once (2^i-1) samples have been fed to the digital filter with the determined difference less than the threshold level.
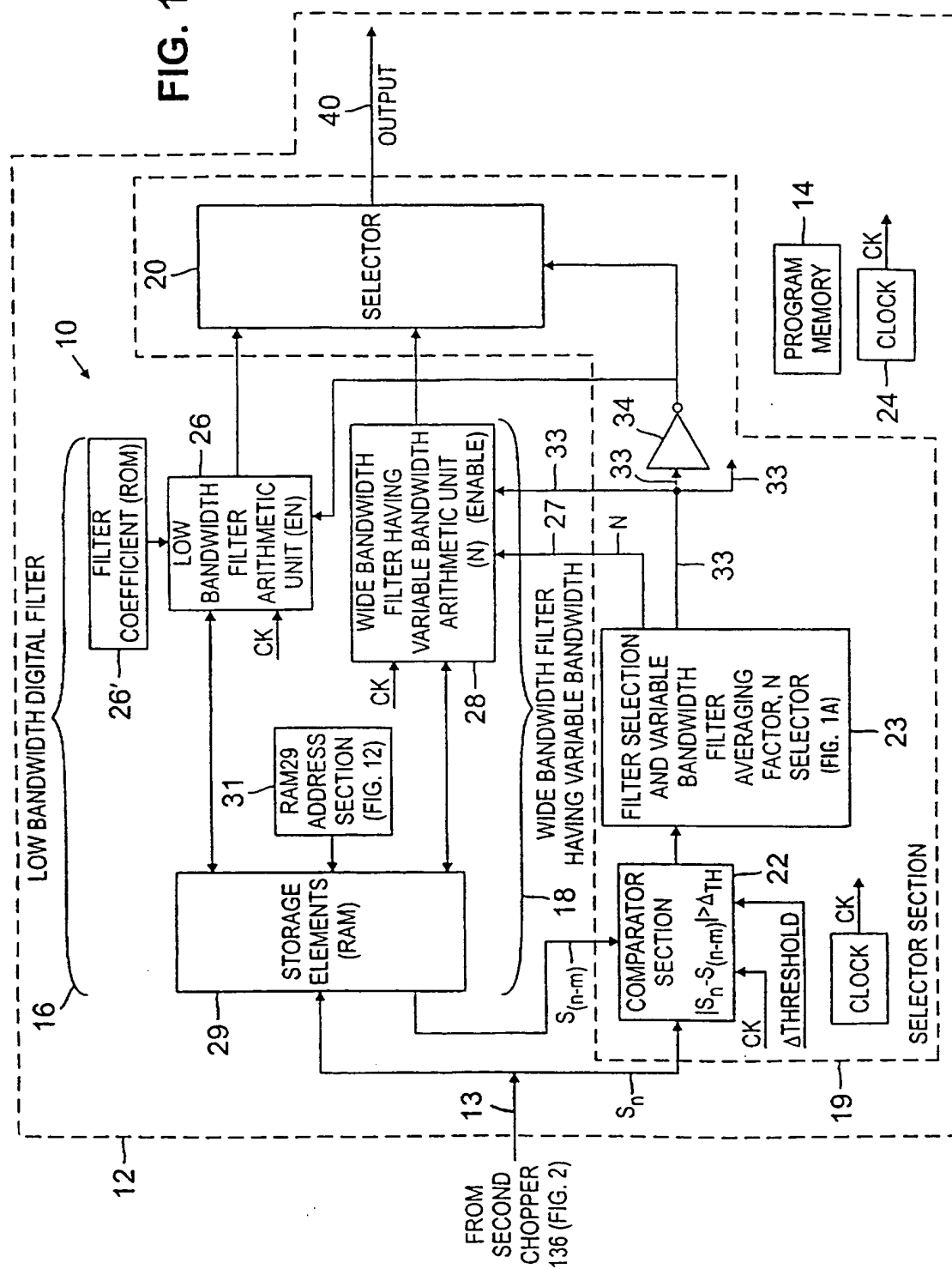
5   22. The system recited in claim 20 wherein N is successively increased by factors of 2 to 2^i once (2^i-1) samples have been fed to the digital filter with the determined difference less than the threshold level.

23. A digital filtering system for processing
10 samples of an input signal, comprising:
a relatively low bandwidth digital filter adapted for coupling to the input signal;
a variable bandwidth digital filter adapted for coupling to the input signal;
15   a selector section for producing output samples from the variable bandwidth filter upon detection of an event and for then producing the output samples from the relatively low bandwidth filter after a predetermined number of samples of the input signal have been processed
20 by the variable bandwidth filter subsequent to the event.

24. The digital filtering system recited in claim 23 wherein the selector section varies the bandwidth of the variable bandwidth filter, such bandwidth being relatively wide upon the detection of the event and then
25 successively reducing until the relatively low bandwidth filter is selected.

25.   The digital filtering system recited in claim
24 wherein one of a plurality of analog input signals is
coupled to the filtering system through a multiplexer and
an analog to digital converter selectively in accordance
5 with a control signal and wherein the event is a change
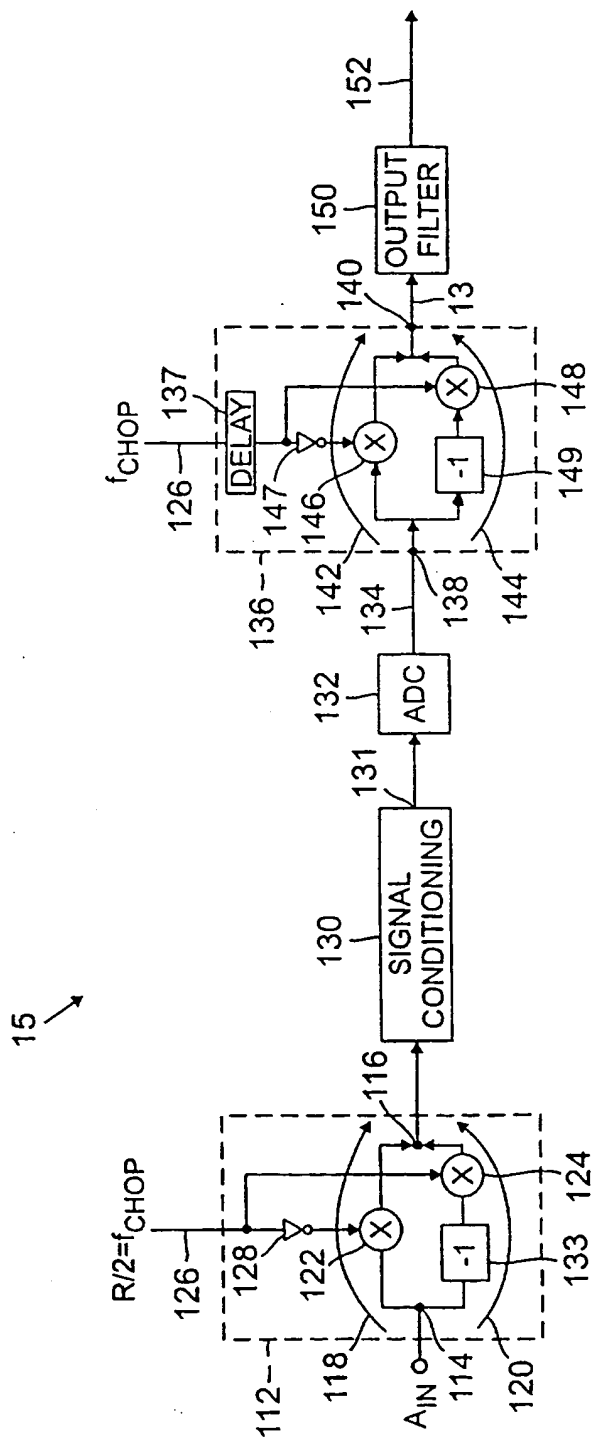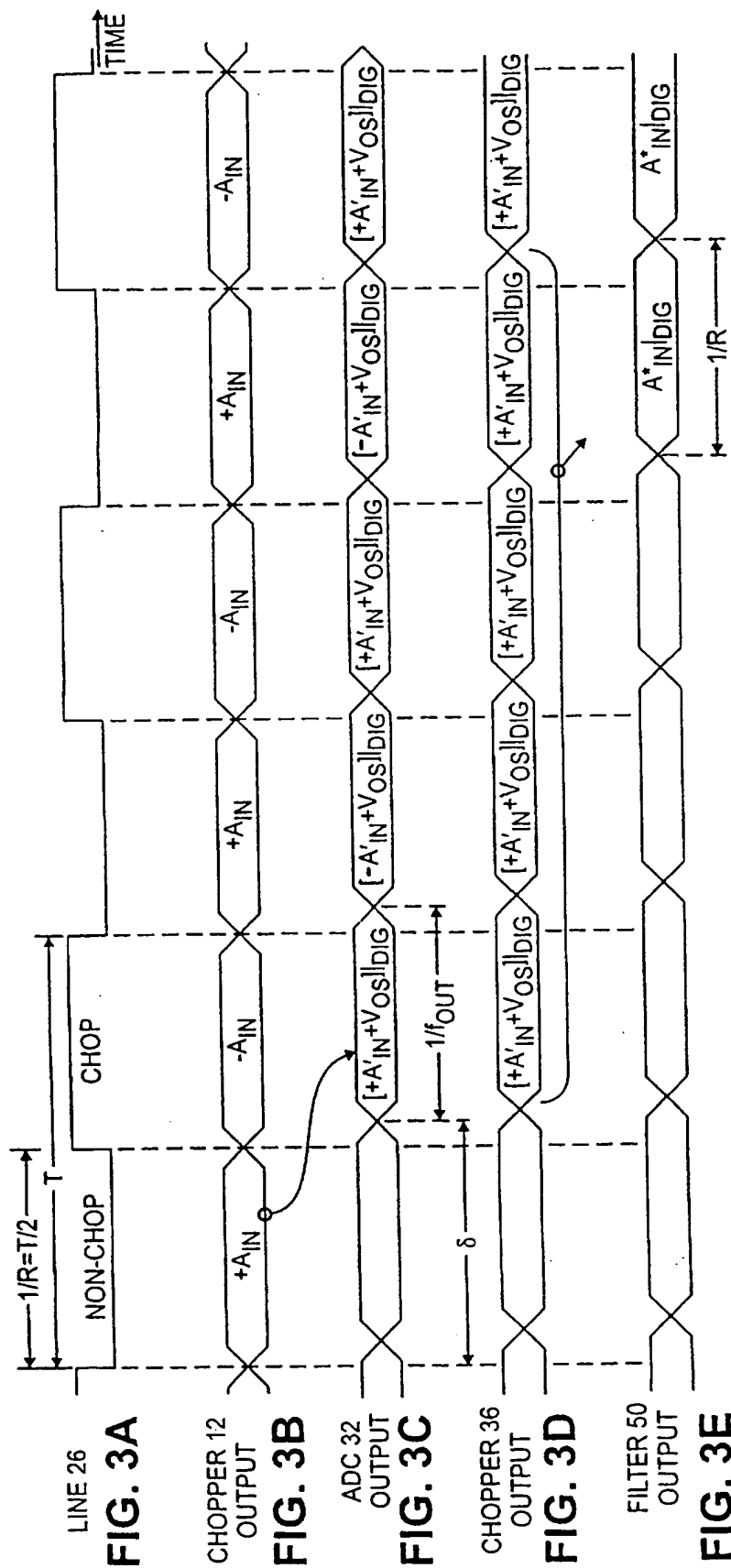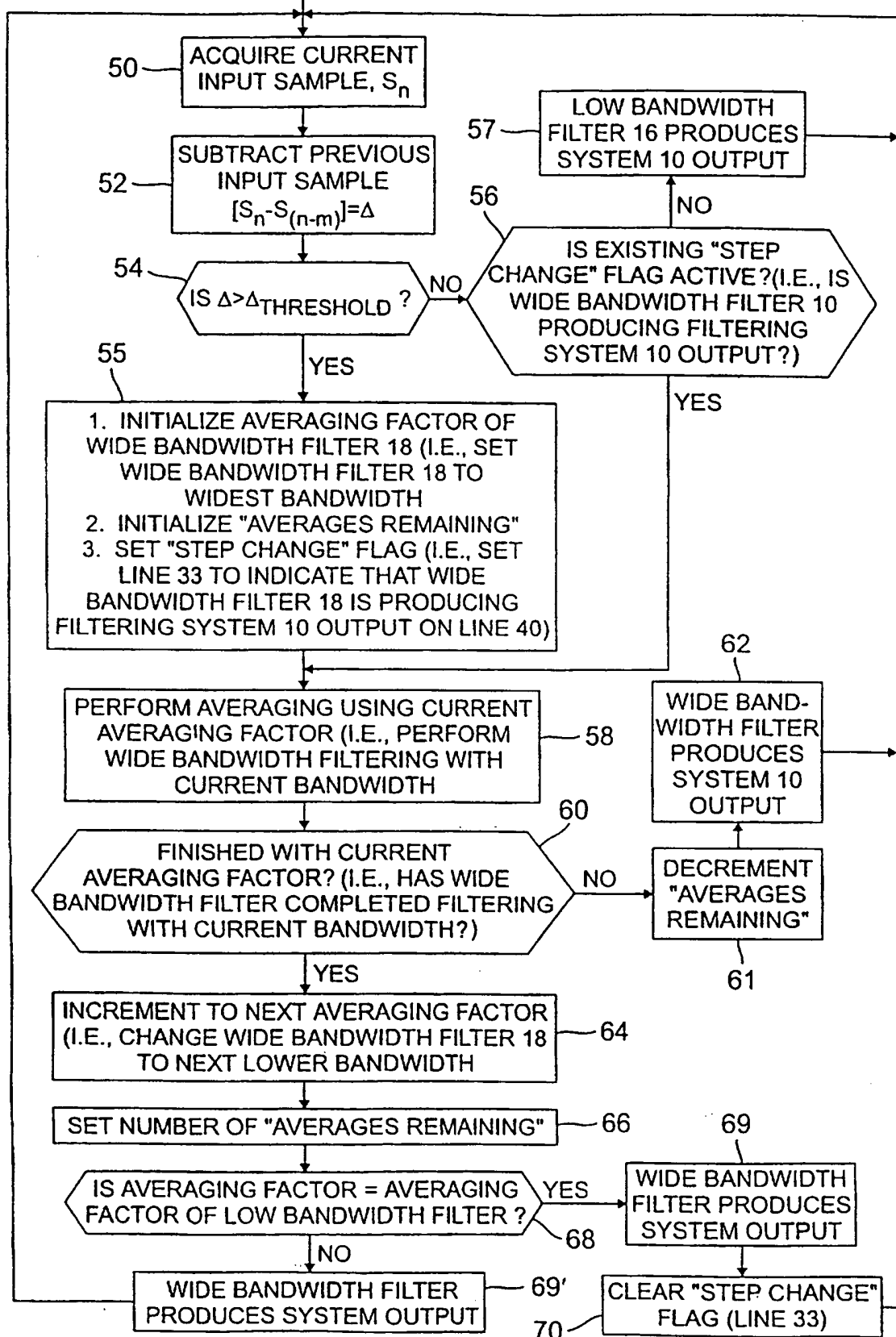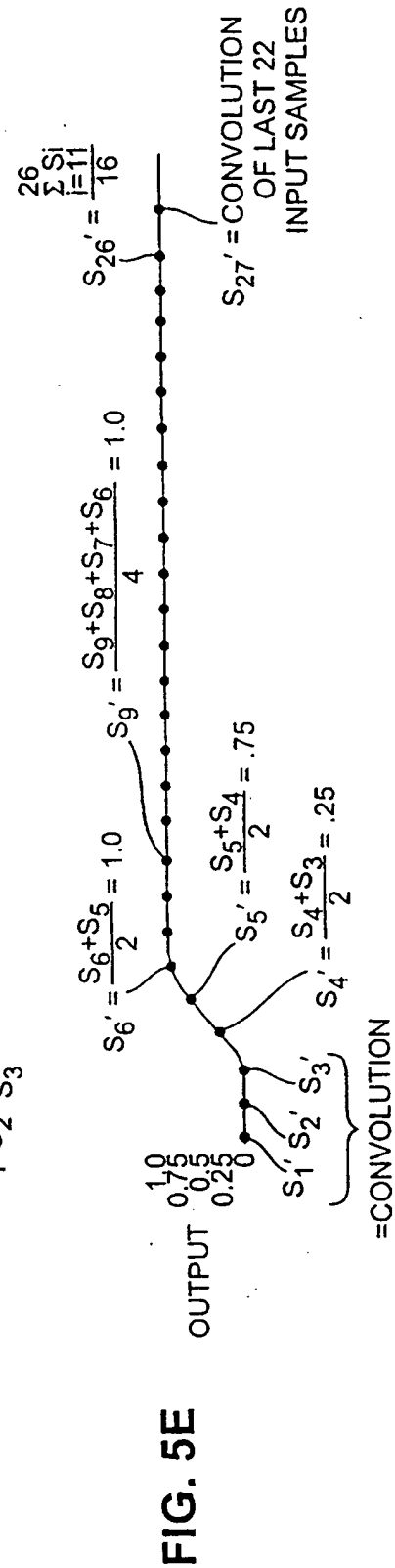in the control signal.

FIG. 1

FIG. 2

FIG. 3A — LINE 26

FIG. 3B — CHOPPER 12 OUTPUT

FIG. 3C — ADC 32 OUTPUT

FIG. 3D — CHOPPER 36 OUTPUT

FIG. 3E — FILTER 50 OUTPUT

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FIG. 4

FIG. 5A

STEP FLAG
(LINE 33)

|← ACTIVE →|

FIG. 5B AVERAGE REMAINING 2 2 2 1 0 3 2 1 0 7 6 5 4 3 2 1 0 5 4 3 2 1 0

FIG. 5C AVERAGE FACTOR 2 2 2 2 2 2 4 4 4 4 8 8 8 8 8 8 16 16 16 16 16 16 F=22

FIG. 5D
INPUT SAMPLES 1 / .5 / 0

S_1 S_2 S_3 S_4 S_5 S_6 S_7 S_8 S_9 S_{10} ... S_{14} ... S_{22} S_{25} S_{26} S_{27}

FIG. 5E
OUTPUT 1.0 / 0.75 / 0.5 / 0.25 / 0

S_1' S_2' S_3' S_4'

=CONVOLUTION

$$S_4' = \frac{S_4 + S_3}{2} = .25$$

$$S_5' = \frac{S_5 + S_4}{2} = .75$$

$$S_6' = \frac{S_6 + S_5}{2} = 1.0$$

$$S_9' = \frac{S_9 + S_8 + S_7 + S_6}{4} = 1.0$$

S_{26}' S_{27}' = CONVOLUTION
OF LAST 22
INPUT SAMPLES

$$S_{26}' = \frac{\sum\limits_{i=11}^{26} S_i}{16}$$

FIG. 6

FIG. 7

FIG. 8

FIG. 9
PRIOR ART

8/9

FIG. 10
PRIOR ART

FIG. 12

OFFSET SELECTION LINES
(E.G. - SUBTRACT 2
- SUBTRACT N)

FIG. 11

SUBSTITUTE SHEET (RULE 26)
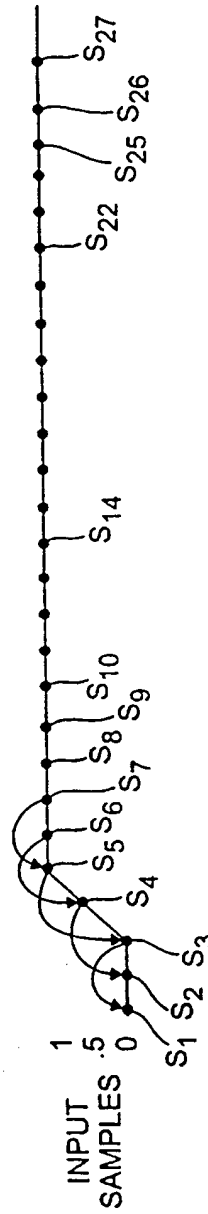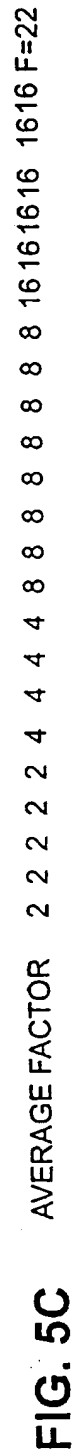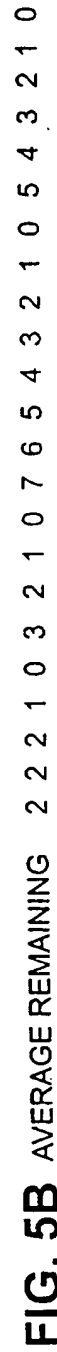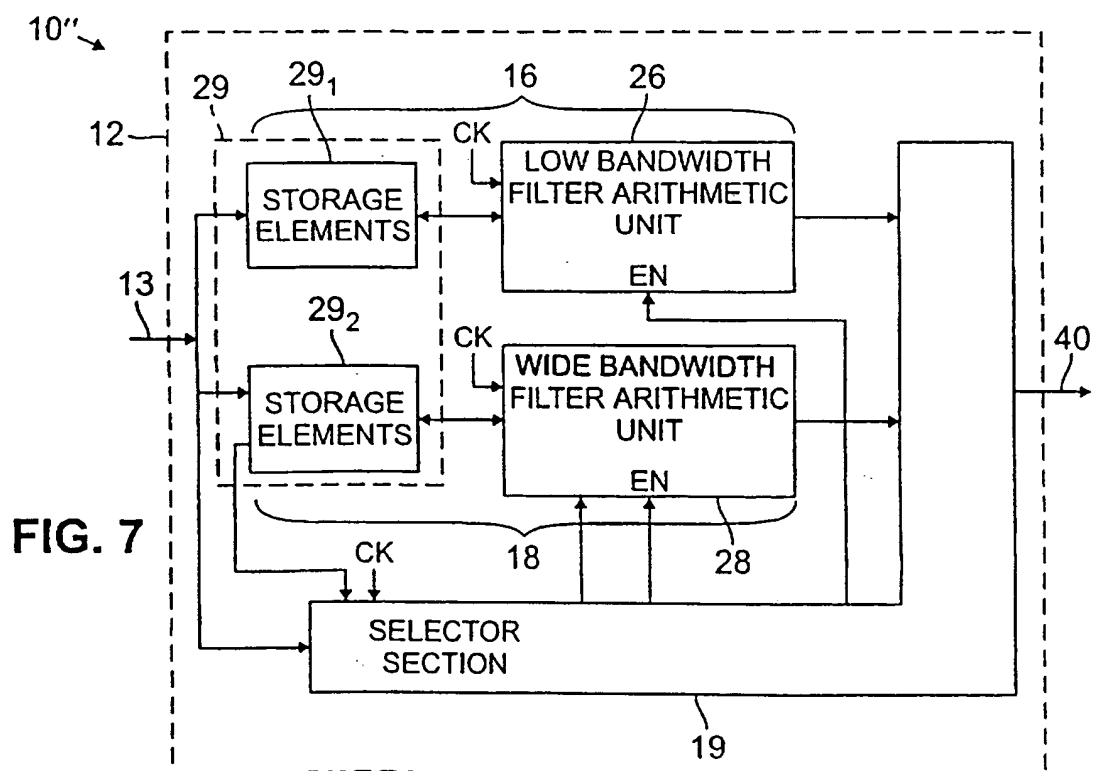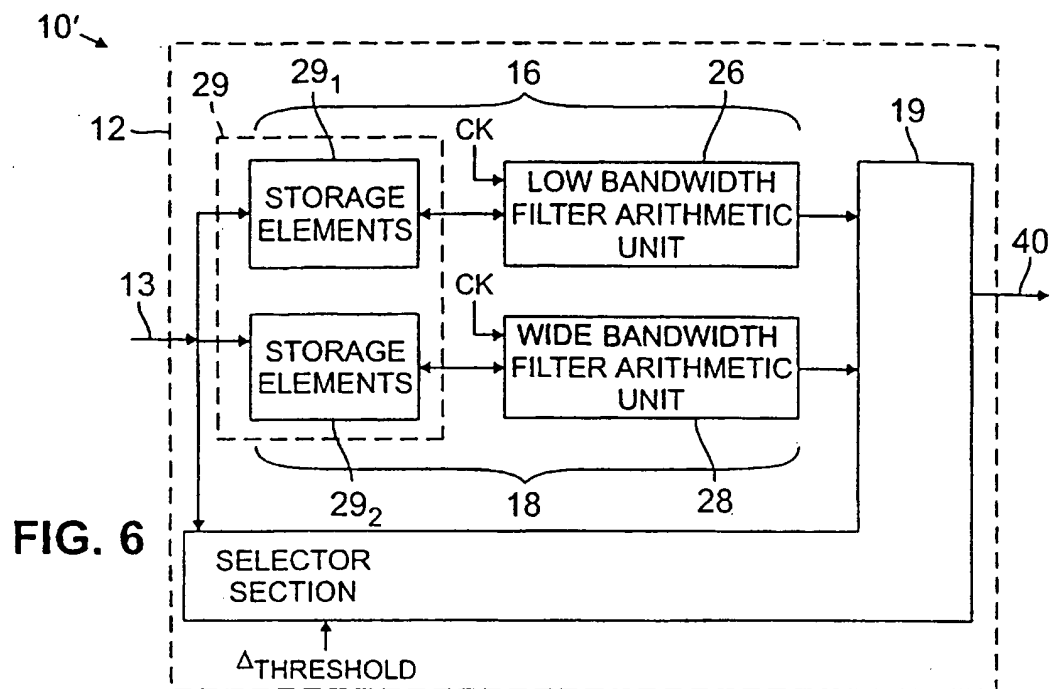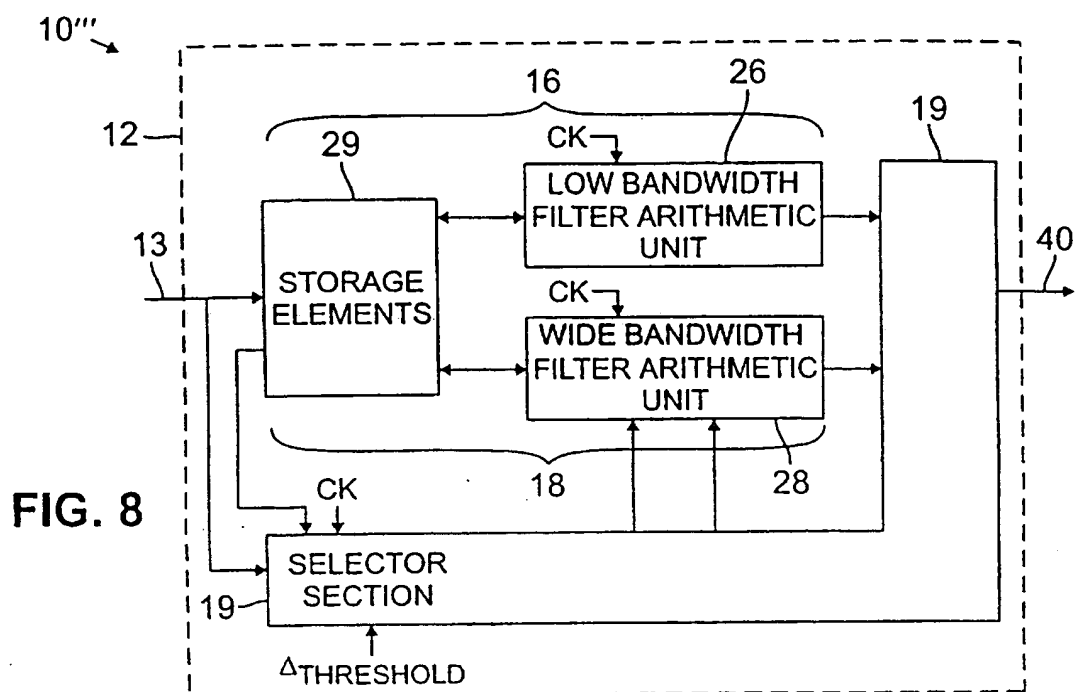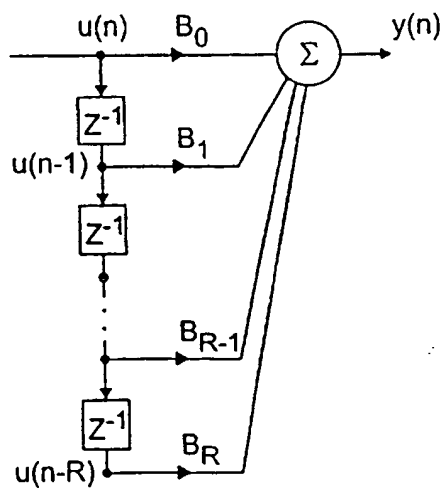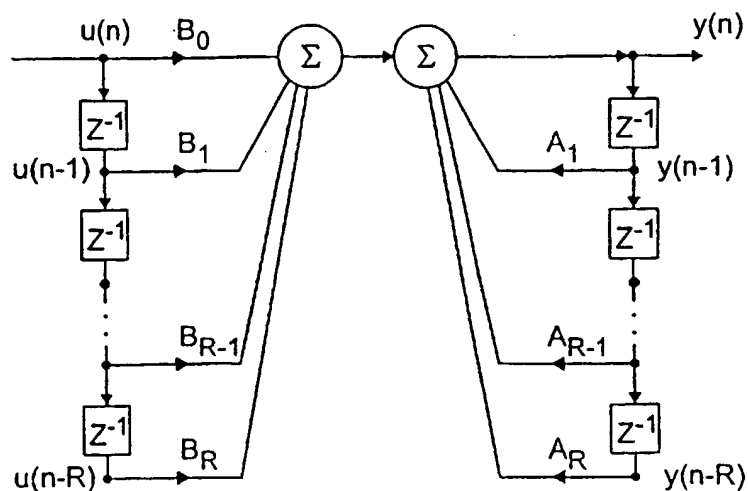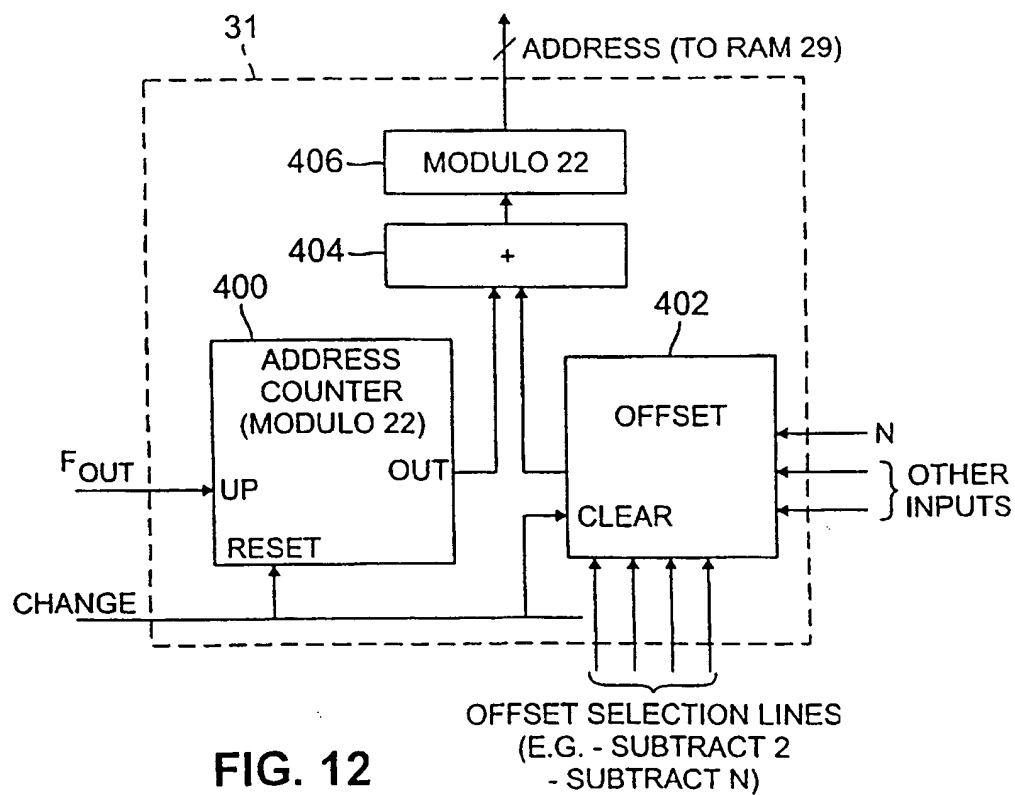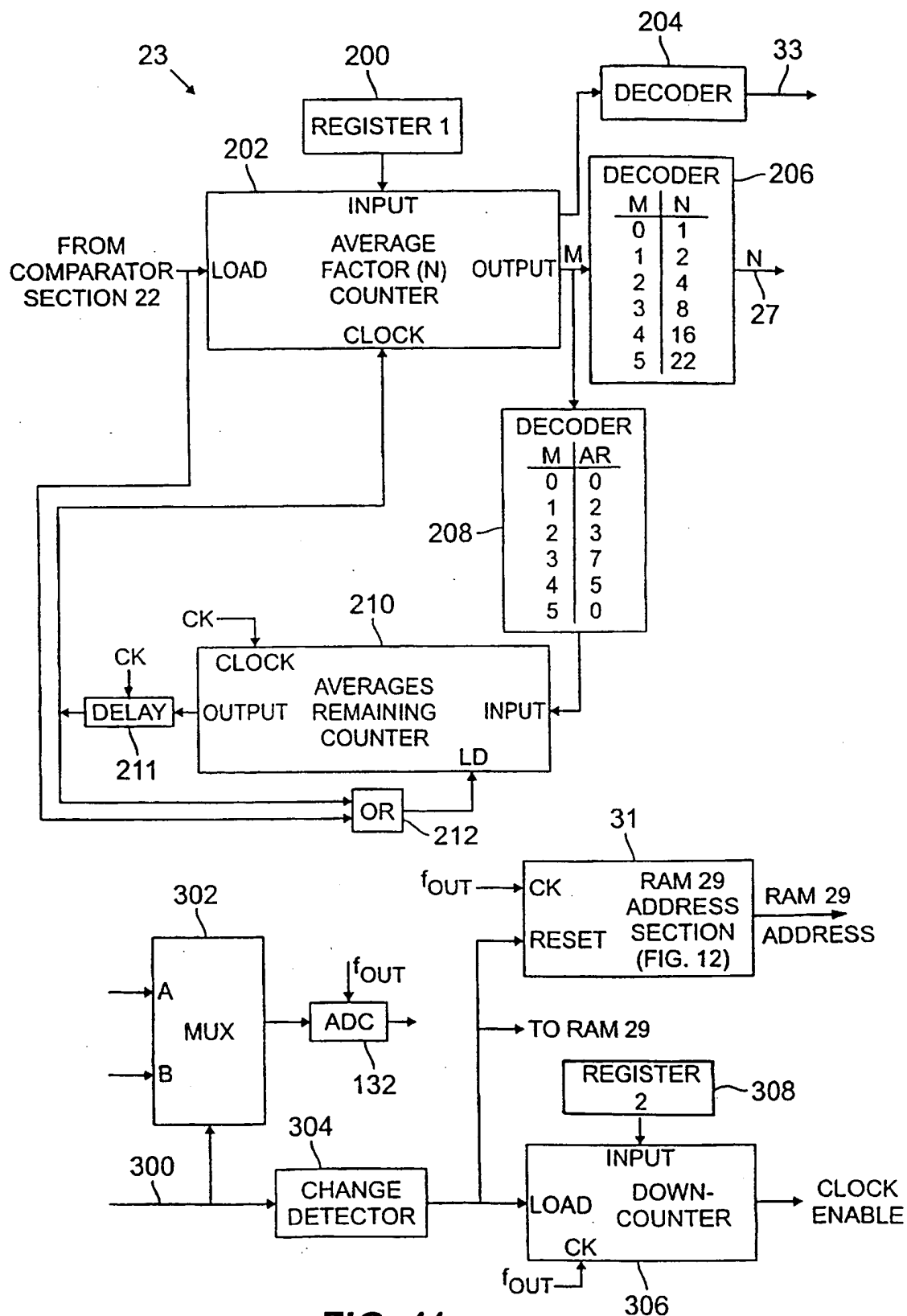
INTERNATIONAL SEARCH REPORT

International application No.

PCT/US97/02222

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :G06F 17/00
US CL   :364/724.13

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. :   364/724.13; 331/17

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y,P	US, A, 5,499,392 (GRUNWELL) 12 March 1996, col. 2 line 28 to col. 3 line 2, col. 5 line 59 to col. 6 line 49, col 7 line 29 to col. 8 line 20, and Figs. 1-6AB.	1-14, 23-25
Y	US, A, 5,408,202 (SHIRAZI ET AL) 18 April 1995, col. 2 line 24 to col. 3 line 15, and Fig. 4.	1-14, 23-25
Y	US, A, 4,771,249 (BURCH ET AL) 13 September 1988, col. 1 line 56 to col. 2 line 18, and Fig.	1-14, 23-25
Y	US, A, 4,506,233 (ENGLUND, JR) 19 March 1985, col. 1 lines 10-25 & 48-53, line 56 to col. 2 line 11, and Fig. 1.	1-14, 23-25

☐ Further documents are listed in the continuation of Box C.   ☐ See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance		
"E"	earlier document published on or after the international filing date	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)		
		"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed	"&"	document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
13 MAY 1997	0 9 JUN 1997

Name and mailing address of the ISA/US	Authorized officer
Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231	TAN V. MAI
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Form PCT/ISA/210 (second sheet)(July 1992)*

BOX II. OBSERVATIONS WHERE UNITY OF INVENTION WAS LACKING
This ISA found multiple inventions as follows:

This application contains the following inventions or groups of inventions which are not so linked as to form a single
inventive concept under PCT Rule 13.1. In order for all inventions to be examined, the appropriate additional
examination fees must be paid.

Group I, claim(s) 1-17 & 23-25 are, drawn to a device having selecting means.
Group II, claim(s) 18-22 are, drawn to a general filter.

The inventions listed as Groups II do not relate to a single inventive concept under PCT Rule 13.1 because, under PCT
Rule 13.2, they lack the same or corresponding special technical features for the following reasons: Group I, claims 1-
17 &23-25 are directed to a digital filter having selecting means for selecting the result of one of two different filters.
Group II, claims 18-22 are directed to a general filter for filtering samples of a input signal.